CLAIMS

What is claimed is:

1. A memory device, comprising:

a memory array;

a register configured to store at least one bit indicating a suspend status of a write operation; and

a control circuit coupled to said memory array and said register, said control circuit configured to update said register and to control the output of a status signal representing said suspend status of said write operation.

2. The memory device of claim 1, wherein said register resides within said control circuit.

3. The memory device of claim 1, wherein said control circuit is configured to receive a status request signal and said register is configured to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

4. The memory device of claim 3, further comprising at least one data input/output coupled to said control circuit, wherein at least one data inputs/output is configured to receive said status request signal from a processor and to provide said status signal to said processor.

5. The memory device of claim 1, further comprising a status output coupled to said register, wherein said status output is configured to

provide a second status signal when said status output is polled, said second status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

6. The memory device of claim 5, wherein said status output represents an output pin.

7. The memory device of claim 1, wherein said write operation represents a byte write operation.

8. The memory device of claim 1, wherein said control circuit includes a first state machine configured to update at least one of said bits indicating said suspend status of said write operation in response to a suspend signal.

9. The memory device of claim 8, wherein said suspend signal represents a byte write suspend command.

10. The memory device of claim 8, wherein said control circuit further includes a second state machine coupled to said first state machine and configured to control the output said status signal in response to a status request signal.

11. The memory device of claim 10, wherein said status request signal is a read status register command.

12. A memory device, comprising:

a memory array;

a register is configured to store at least one bit indicating a protection status of a data modification operation; and

a control circuit coupled to said memory array and said register, said control circuit is configured to update said register and to control the output of a status signal representing said protection status of said data modification operation.

13. The memory device of claim 12, wherein said register resides within said control circuit.

14. The memory device of claim 12, wherein said control circuit is configured to receive a status request signal and said register is configured to output said status signal in response to said status request signal, said status signal having a first state to indicate said data modification operation attempted to access at least one memory location within a protected memory block and a second state to indicate said data modification operation accessed at least one of said memory locations within an unprotected memory block.

15. The memory device of claim 14, further comprising at least one data input/output coupled to said control circuit, wherein at least one data inputs/output is configured to receive said status request signal from a processor and to provide said status signal to said processor.

16. The memory device of claim 12, wherein said data modification operation is a programming operation or an erase operation.

17. The memory device of claim 12, wherein said control circuit includes a first state machine configured to update at least one of said bits indicating said protection status of said data modification operation in response to a block lock configuration signal.

18. The memory device of claim 17, wherein said block lock configuration signal includes a set block lock bit command.

19. The memory device of claim 18, wherein said control circuit further includes a second state machine coupled to said first state machine and configured to control the output said status signal in response to a status request signal.

20. A method of providing the suspend status of a programming operation in a memory device, comprising the steps of:

(a) performing a programming operation to a first memory location;

(b) prior to the completion of said programming operation, receiving a suspend signal;

(c) determining whether or not to suspend said programming operation;

(d) if said programming operation is suspended, updating, if necessary, a status register to indicate said programming operation is suspended; and

(e) providing an output signal to indicate said suspend status of programming operation.

21. The method of claim 20, wherein step (e) comprises the steps of:

(1) receiving a read status register signal; and

(2) providing said output signal in response to said read status register signal.

22. The method of claim 20, wherein step (e) comprises the step of providing said output signal at a dedicated status output.

23. The method of claim 20, further comprising the steps of:

(f) performing a second data modification operation to a second memory location;

(g) after the completion of said second data modification operation, updating, if necessary, said status register to indicate said write operation is not suspended; and

(h) resuming said first data modification operation.

24. The method of claim 23, wherein said second data modification operation is a read operation.

25. The method of claim 20, further comprising, prior to step (a), the step of:

(f) initializing said status register to indicate said write operation is not suspended.

26. A method of providing the protection status of a data modification operation in a memory device, comprising the steps of:

(a) performing a data modification operation to a memory location;

(b) determining said protection status of said memory location;

(c) providing an output signal to indicate said protection status of said memory location.

27. The method of claim 26, wherein step (c) comprises the steps of:

(1) receiving a read status signal; and

(2) providing said output signal in response to said read status signal.

28. The method of claim 26, further comprising, prior to step (a), the step of:

(d) initializing a status register to indicate said memory location is protected from data modifications.

29. The method of claim 26, wherein step (b) comprises the steps of:

(1) performing a read operation to a location within a block lock memory array that corresponds to said memory location; and

(2) updating a status register.

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